ABSTRACT

According to the invention, a JTAG-compliant chip is further provided with a controller that receives data provided on the TDI input pin, forms parallel address and data instructions and passes the data through IO pins to the non-JTAG chip without requiring the data to go through the boundary scan register chain of the JTAG-compliant chip. This controller is used to program, erase, and read the other chip. For a non-JTAG flash memory device, the controller in the JTAG-compliant chip generates the necessary programming signal sequences, and applies them to the non-JTAG chip without going through the JTAG boundary scan circuitry.